Claims

We claim:

1. A mixed-signal core designed for efficient testing, comprising:

an analog module having a plurality of analog components and a plurality of mixed-signal components;

a first digital module having a first plurality of digital components required for functional/parametric verification of the plurality of mixed-signal components within the analog module;

a first virtual boundary coupled between the analog module and the first digital module, the first virtual boundary having at least one multiplexer to gate a plurality of signals transmitted between the analog module and the digital module, wherein the first virtual boundary partitions the analog module from the digital module, each of the at least one multiplexer coupled to receive the plurality of signals generated by the plurality of analog and the plurality of mixed-signal components of the analog module and the first plurality of digital components of the digital module;

a second digital module having a second plurality of digital components; and

a second virtual boundary having at least one multiplexer to gate a plurality of signals transmitted between the first and the second digital module, wherein the second virtual boundary partitions the first digital module from the second digital module, each of the at least one multiplexer coupled to receive the plurality of signals generated by the first plurality of digital components and the second plurality of digital components;

wherein the structure for testing has at least three modes of operation for testing the mixed signal core, a first mode of operation that provides digital interface characterization testing of the first and second digital module and analog characterization/trimming testing of the analog module, wherein, in the first mode of operation, the first virtual boundary and the second virtual boundary are inactive;

wherein a second mode of operation that provides concurrent testing of the analog module, the first digital module, and the second digital module, wherein analog characterization/trimming testing is performed on the analog module and digital interface characterization testing is performed on the first digital module, while SCAN/BIST testing is performed on the second digital module, wherein, in the second mode of operation, the second virtual boundary is activated to gate the plurality of signals transmitted between the first digital module and the second digital module;

wherein a third mode of operation that provides non-concurrent testing of the analog module, the first digital module, and the second digital module, the third mode of operation supplies SCAN/BIST testing of the first and second plurality of digital components from the first digital module and the second digital module, while the analog module is powered down, and wherein, in the third mode of operation, the first and second virtual boundaries are activated to gate the plurality of signals transmitted between the first digital module and the analog module and to gate the plurality of signals transmitted between the first digital module and the second digital module, respectively.

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2. A structure for testing an integrated circuit chip having an analog core, a mixed-signal core, a digital core, a microprocessor core, and a memory core therein, comprising:

wherein the mixed-signal core comprises,

an analog module having a plurality of analog components and a plurality of mixed-signal components,

a first digital module having a first plurality of digital components required for functional/parametric verification of the plurality of mixed-signal components within the partitioned analog module,

a first virtual boundary coupled between the analog module and the first digital module, the first virtual boundary having at least one multiplexer to gate a plurality of signals transmitted between the analog module and the digital module, wherein the first virtual boundary partitions the analog module from the digital module, each of the at least one multiplexer coupled to receive the plurality of signals generated by the plurality of analog and the plurality of mixed-signal components of the analog module and the first plurality of digital components of the digital module,

a second digital module having a second plurality of digital components, and

a second virtual boundary having at least one multiplexer to gate a plurality of signals transmitted between the first and the second digital module, wherein the second virtual boundary partitions the first digital module from the second digital module, each of the at least one multiplexer coupled to receive the plurality of signals generated by the first plurality of digital components and the second plurality of digital components;

wherein the structure for testing has at least three modes of operation for testing the mixed-signal core, a first mode of operation that provides digital interface characterization testing of the first and second digital module and analog characterization/trimming testing of the analog module, wherein, in the first mode of operation, the first virtual boundary and the second virtual boundary are inactive;

wherein a second mode of operation that provides concurrent testing of the analog module, the first digital module, and the second digital module, wherein analog characterization/trimming testing is performed on the analog module and digital interface characterization testing is performed on the first digital module, while SCAN/BIST testing is performed on the second digital module, wherein, in the second mode of operation, the second virtual boundary is activated to gate the plurality of signals transmitted between the first digital module and the second digital module;

wherein a third mode of operation that provides non-concurrent testing of the analog module, the first digital module, and the second digital module, the third mode of operation supplies SCAN/BIST testing of the first and second plurality of digital components from the first digital module and the second digital module, while the analog module is powered down, and wherein, in the third mode of operation, the first and second virtual boundaries are activated to gate the plurality of signals transmitted between the first digital module and the analog module and to gate the plurality of signals transmitted between the first digital module and the second digital module, respectively;

wherein the microprocessor core for executing microprocessor instructions multiple times and evaluating the results to ensure integrity of the microprocessor core and for testing the memory core by generating a memory test pattern by the memory core and evaluating the results; and

a host computer for providing an executable test program to the microprocessor core through an interface circuit;

wherein the analog module and the first digital module are provided with a test pattern for characterization testing generated by the microprocessor core and the resultant output of the analog module and the first digital module are evaluated by either the microprocessor core or the host computer;

wherein the first and second digital module are provided with a test pattern for SCAN/BIST testing generated by the microprocessor core and the resultant output of the first and second digital module are evaluated by either the microprocessor core or the host computer.

3. A structure for testing a integrated circuit chip as recited in claim 2, wherein the test program applied to the microprocessor core is an object code of assembly language test program.

4. A structure for testing a integrated circuit chip as recited in claim 3, wherein the assembly language test program is provided to the microprocessor core from an external host computer through an I/O interface.

5. A structure for testing a integrated circuit chip as recited in claim 3, wherein the assembly language test program is provided to the microprocessor core from an external IC tester through an I/O interface.

6. A structure for testing a integrated circuit chip as recited in claim 2, wherein the integrated circuit chip is a system-on-chip (SoC) IC.

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7. A mixed-signal core designed for efficient testing, comprising:

an analog module having a plurality of analog components and a plurality of mixed-signal components,

a first digital module coupled to the analog module, the first digital module having a first plurality of digital components required for functional/parametric verification of the plurality of mixed-signal components within the partitioned analog module, wherein the first digital module provides a plurality of clocking signals, a power-down control signal, a reset signal, an analog test sequence to the analog module,

a first isolation unit including a first plurality of multiplexers, the first isolation unit coupled between the analog module and the first digital module to form a first virtual boundary that isolates a plurality of signals between the analog module and the first digital module,

a second digital module having a second plurality of digital components,

a second isolation unit coupled between the first digital module and the second digital module to form a second virtual boundary that isolates a plurality of signals between the first digital module and the second digital module,

a partition controller coupled to the first and second digital module to provide a test clock control signal, a SCAN enable control signal, a Built-in self test (BIST) control signal and a mixed-signal parallel test control signal,

a testing clock signal generator coupled between the partition controller and the first digital module to provide a clocking signal for the first digital module,

a top level pin multiplexing unit coupled to the analog module, the first digital module, and the second digital module, to multiplex serial data internal to the integrated circuit, and

a data multiplexer coupled to the top level pin multiplexing unit, the first digital module and the second digital module, wherein the structure for testing has at least three modes of operation for testing the mixed-signal core, a first mode of operation that provides digital interface characterization testing of the first and second digital module and analog characterization/trimming testing of the analog module, wherein, in the first mode of operation, the first isolation unit and the second isolation unit are inactive;

wherein a second mode of operation that provides concurrent testing of the analog module, the first digital module, and the second digital module, wherein analog characterization/trimming testing is performed on the analog module and digital interface characterization testing is performed on the first digital module, while SCAN/BIST testing is performed on the second digital module, wherein, in the second mode of operation, the second isolation unit is activated to gate the plurality of signals transmitted between the first digital module and the second digital module;

wherein a third mode of operation that provides non-concurrent testing of the analog module, the first digital module, and the second digital module, the third mode of operation supplies SCAN/BIST testing of the first and second plurality of digital components from the first digital module and the second digital module, while the analog module is powered down, and wherein, in the third mode of operation, the first and second isolation units are activated to gate the plurality of signals transmitted between the first digital module and the analog module and to gate the plurality of signals transmitted between the first digital module and the second digital module, respectively.

8. A structure for testing an integrated circuit chip having an analog core, an mixed-signal core, an digital core, a microprocessor core, and a memory core therein, comprising:

wherein the mixed-signal core comprises,

an analog module having a plurality of analog components and a plurality of mixed-signal components,

a first digital module coupled to the analog module, the first digital module having a first plurality of digital components required for functional/parametric verification of the plurality of mixed-signal components within the partitioned analog module, wherein the first digital module provides a plurality of clocking signals, a power-down control signal, a reset signal, an analog test sequence to the analog module,

a first isolation unit including a first plurality of multiplexers, the first isolation unit coupled between the analog module and the first digital module to form a first virtual boundary that isolates a plurality of signals between the analog module and the first digital module,

a second digital module having a second plurality of digital components,

a second isolation unit coupled between the first digital module and the second digital module to form a second virtual boundary that isolates a plurality of signals between the first digital module and the second digital module,

a partition controller coupled to the first and second digital module to provide a test clock control signal, a SCAN enable control signal, a Built-in self test (BIST) control signal and a mixed-signal parallel test control signal,

a testing clock signal generator coupled between the partition controller and the first digital module to provide a clocking signal for the first digital module,

a top level pin multiplexing unit coupled to the analog module, the first digital module, and the second digital module, to multiplex serial data internal to the integrated circuit, and

a data multiplexer coupled to the top level pin multiplexing unit, the first digital module and the second digital module,

wherein the structure for testing has at least three modes of operation for testing the mixed-signal core, a first mode of operation that provides digital interface characterization testing of the first and second digital module and analog characterization/trimming testing of the analog module, wherein, in the first mode of operation, the first isolation unit and the second isolation unit are inactive;

wherein a second mode of operation that provides concurrent testing of the analog module, the first digital module, and the second digital module, wherein analog characterization/trimming testing is performed on the analog module and digital interface characterization testing is performed on the first digital module, while SCAN/BIST testing is performed on the second digital module, wherein, in the second mode of operation, the second isolation unit is activated to gate the plurality of signals transmitted between the first digital module and the second digital module;

wherein a third mode of operation that provides non-concurrent testing of the analog module, the first digital module, and the second digital module, the third mode of operation supplies SCAN/BIST testing of the first and second plurality of digital components from the first digital module and the second digital module, while the analog module is powered down, and wherein, in the third mode of operation, the first and second isolation units are activated to gate the plurality of signals transmitted between the first digital module and the analog module and to gate the plurality of signals transmitted between the first digital module and the second digital module, respectively;

wherein the microprocessor core for executing microprocessor instructions multiple times and evaluating the results to ensure integrity of the microprocessor core and for testing the memory core by generating a memory test pattern by the memory core and evaluating the results; and

a host computer for providing an executable test program to the microprocessor core through an interface circuit;

wherein the analog module and the first digital module are provided with a test pattern for characterization testing generated by the microprocessor core and the resultant output of the analog module and the first digital module are evaluated by either the microprocessor core or the host computer;

wherein the first and second digital module are provided with a test pattern for SCAN/BIST testing generated by the microprocessor core and the resultant output of the first and second digital module are evaluated by either the microprocessor core or the host computer.

9. A structure for testing a integrated circuit chip as recited in claim 8, wherein the first isolation unit comprises,

a clock/power-down multiplexer coupled between to the first digital module and the analog module, the first clock/power-down multiplexer coupled to receive the clocking signal from the first digital module and a mixed-signal parallel test control signal;

a digital-to-analog converter (DAC) data multiplexer coupled between the first digital module and the analog module, the DAC data multiplexer coupled to receive the mixed-signal parallel test control signal and data from the first digital module; and

an analog-to-digital converter (ADC) data multiplexer coupled between the first digital module and the analog module, the ADC data multiplexer coupled to receive the mixed-signal parallel test control signal and data from the analog module.

10. A structure for testing a integrated circuit chip as recited in claim 8, wherein the second isolation unit comprises,

a serial-to-parallel data converter coupled to receive serial data from the second digital module;

a format converter/post processing unit coupled to the serial-to-parallel converter to format and process the parallel data;

at least one multiplexer coupled to the format converter/post processing unit, the first digital module, and the second digital module to provide an isolated control interface, the at least one multiplexer coupled to receive the mixed-signal parallel test control signal from the partition controller.

11 . A structure for testing a integrated circuit chip as recited in claim 8, wherein the testing clock signal generator comprises,

a digital clock controller;

a top level clock controller coupled to the partition controller; and a clock multiplexer, having a first input, a second input, a control input, and an output, to provide a multiplexed clocking signal to the first digital module, the first input coupled to the top level clock controller, the second input coupled to the digital clock controller, the control input coupled to the partition controller, the output coupled to the first digital module.

12. A structure for testing a integrated circuit chip as recited in claim 8, wherein the test program applied to the microprocessor core is an object code of assembly language test program.

13. A structure for testing a integrated circuit chip as recited in claim 8, wherein the assembly language test program is provided to the microprocessor core from an external host computer through an I/O interface.

14. A structure for testing a integrated circuit chip as recited in claim 8, wherein the assembly language test program is provided to the microprocessor core from an external IC tester through an I/O interface.

15. A structure for testing a integrated circuit chip as recited in claim 8, wherein the integrated circuit chip is a system-on-chip (SoC) IC.